

Appl. No. 10/757,302  
Reply to Advisor/Action of March 30, 2006

Attorney Docket No. 2002-0350/24061.484  
Customer No. 42717

**Amendments To The Claims**

Please cancel Claims 15-19 without prejudice. The following list of the claims replaces all prior versions and lists of the claims in this application.

1. (Previously presented) A method for the planarization of an integrated circuit structure comprising:

providing a substrate having a plurality of patterned regions;

polishing said substrate with an initial chemical mechanical polishing slurry until partial planarization occurs; and

continuing to final planarization with a second slurry;

wherein said initial slurry comprises a diluted ceria-based slurry with the compositions that ranges from 0.5 wt. % to 1.0 wt. % ceria; and

wherein said second slurry comprises a ceria-based slurry with composition ranging from 1.0 wt. % to 2.0 wt. % ceria, said initial slurry and said second slurry having different concentrations of ceria.

2. (Original) The method of claim 1 wherein said integrated circuit structure comprises shallow trench isolation.

3. (Original) The method of claim 2 wherein said shallow trench isolation comprises silicon oxide, silicon nitride and polysilicon layers in various configurations.

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4. (Cancelled).

5. (Cancelled).

6. (Original) The method of claim 1 wherein said polishing said substrate with said initial chemical mechanical polishing slurry until partial planarization occurs comprises a control of polishing time so as to avoid overpolishing of a stop layer.

7. (Cancelled).

8. (Original) The method of claim 1 wherein said continuing to final planarization with said second slurry completes said planarization.

9. (Previously presented) A method for the planarization of an integrated circuit structure comprising:

providing a substrate having a plurality of patterned regions wherein said substrate is to be planarized to a stop layer;

polishing said substrate with a first chemical mechanical polishing slurry composition until partial planarization occurs; and

thereafter continuing to final planarization with a second slurry;

wherein said first slurry comprises a diluted ceria-based slurry with compositions ranging from 0.5 wt. % to 1.0 wt. % ceria

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wherein said second slurry comprises a ceria-based slurry with composition ranging from 1.0 wt. % to 2.0 wt. % ceria, said first and second slurries having different concentrations of ceria.

10. (Original) The method of claim 9 wherein said integrated circuit structure comprises shallow trench isolation comprising silicon oxide and wherein said stop layer comprises one or more silicon nitride or polysilicon layers.

11. (Cancelled).

12. (Cancelled).

13. (Original) The method of claim 9 wherein said polishing said substrate with said first chemical mechanical polishing slurry composition until partial planarization occurs further comprises a control of polishing time so as to avoid overpolishing of said stop layer.

14. (Cancelled).

15. (Cancelled).

16. (Cancelled).

17. (Cancelled).

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18. (Cancelled).

19. (Cancelled).